CLAIMS

1. A method of refreshing dynamic data stored in an integrated circuit, the integrated circuit being adapted to receive a supply voltage and being adapted to operate in a self-refresh mode of operation to refresh the dynamic data at a refresh time that defines how often the dynamic data is refreshed during the self-refresh mode, the method comprising monitoring a magnitude of the supply voltage and adjusting the refresh time as a function of the monitored magnitude of the supply voltage.

2. The method of claim 1 wherein adjusting the refresh time as a function of the monitored magnitude of the supply voltage comprises decreasing the refresh time as the magnitude of the supply voltage decreases to refresh the dynamic data more frequently.

3. The method of claim 2 wherein decreasing the refresh time as the magnitude of the supply voltage decreases comprises linearly increasing a frequency of a self-refresh clock signal, the self-refresh clock signal defining the refresh time.

4. The method of claim 1 wherein monitoring the magnitude of the supply voltage comprises detecting whether the magnitude is less than or equal to a minimum supply voltage.

5. The method of claim 4 wherein adjusting the refresh time as a function of the monitored magnitude of the supply voltage comprises reducing the refresh time once the supply voltage has been detected as being less than or equal to the minimum supply voltage.

6. The method of claim 1 wherein monitoring the magnitude of the supply voltage comprises detecting whether the supply voltage is less than or equal to a minimum supply voltage, and adjusting the refresh time as a function of the monitored magnitude of the

supply voltage comprises maintaining the refresh time substantially constant until the supply voltage is less than or equal to the minimum supply voltage, and decreasing the refresh time as a function of decreases in the supply voltage once the detected supply voltage is less than or equal to the minimum supply voltage.

7. The method of claim 6 wherein decreasing the refresh time as a function decreases in the supply voltage once the detected supply voltage is less than or equal to the minimum supply voltage comprises generating a bias voltage from the supply voltage, the bias voltage having a value that is inversely related to the refresh time, and increasing the bias voltage as a function of decreases in the supply voltage once the detected supply voltage is less than or equal to the minimum supply voltage.

8. The method of claim 1 wherein monitoring the magnitude of the supply voltage comprises detecting whether the supply voltage is less than or equal to a minimum supply voltage, and adjusting the refresh time as a function of the monitored magnitude of the supply voltage comprises generating a refresh time adjustment command that determines a value of the refresh time, the value being a function of the detected supply voltage, and setting the refresh time to the determined value.

9. The method of claims 8 wherein generating a refresh time adjustment command comprises generating the command external to the integrated circuit and applying the command to the integrated circuit, and setting the refresh time to the determined value comprises decoding the applied command and adjusting the refresh time to the value corresponding to the decoded command.

10. A method of refreshing dynamic data stored in an integrated circuit, the integrated circuit being adapted to receive a supply voltage and including a refresh oscillator that generates a refresh clock signal having a frequency that is a function of a bias voltage, the bias

voltage being derived from the supply voltage and the integrated circuit being adapted to operate in a self-refresh mode of operation to refresh the dynamic data at a refresh rate that is a function of the frequency of the refresh clock signal, the method comprising monitoring the supply voltage and controlling the bias voltage as a function of the monitored supply voltage.

11. The method of claim 10 wherein controlling the bias voltage as a function of the monitored supply voltage comprises maintaining the bias voltage substantially constant when the supply voltage is greater than a minimum supply voltage, and adjusting the bias voltage as the supply voltage decreases when the supply monitored supply voltage is less than or equal to the minimum supply voltage.

12. The method of claim 11 wherein monitoring the supply voltage comprises detecting whether the supply voltage is less than or equal to a minimum supply voltage, and controlling the bias voltage as a function of the monitored supply voltage comprises maintaining the bias voltage substantially constant when the supply voltage is greater than the minimum supply voltage and adjusting the bias voltage to increase the frequency of the refresh clock signal as a linear function of decreases in the supply voltage when the detected supply voltage is less than or equal to the minimum supply voltage.

13. The method of claim 10 wherein controlling the bias voltage as a function of the monitored supply voltage comprises maintaining the bias voltage substantially constant when the supply voltage is greater than a minimum supply voltage and applying the supply voltage as the bias voltage when the supply voltage is less than or equal to the minimum supply voltage.

14. The method of claim 10 wherein controlling the bias voltage as a function of the monitored supply voltage comprises maintaining the bias voltage substantially constant when the supply voltage is greater than a first minimum supply voltage, and adjusting the bias

voltage to increase the frequency of the refresh clock signal as a function of decreases in the supply voltage when the supply voltage is less than or equal to the first minimum supply voltage and greater than a second minimum supply voltage, and applying the supply voltage as the bias voltage when the supply voltage is less than or equal to the second minimum supply voltage.

15. The method of claim 10 wherein monitoring the supply voltage comprises detecting whether the supply voltage is less than or equal to a minimum supply voltage, and controlling the bias voltage as a function of the monitored supply voltage comprises generating a bias voltage adjustment command, the command having a first value that maintains the bias voltage substantially constant when the supply voltage is greater than the minimum supply voltage, and generating the bias voltage adjustment command having a second value when the supply voltage is less than or equal to the minimum supply voltage, and adjusting the bias voltage as a function of the supply voltage when the command has the second value.

16. The method of claims 15 wherein generating a bias voltage adjustment command comprises generating the bias voltage adjustment command external to the integrated circuit and applying the command to the integrated circuit, and adjusting the bias voltage as a function of the supply voltage when the bias voltage adjustment command has the second value comprises decoding the applied bias voltage adjustment command and thereafter adjusting the bias voltage as the supply voltage varies.

17. A refresh controller for controlling a refresh rate of dynamic data, the refresh controller being adapted to receive a supply voltage and including a refresh oscillator that generates a refresh clock signal having a frequency that is a function of a bias voltage, the refresh circuit operable in a normal mode when the supply voltage is greater than a minimum value to apply a substantially constant bias voltage to the refresh oscillator and to generate refresh signals in response to the corresponding refresh clock signal, the refresh signals defining a first refresh rate having a value determined by the frequency of the refresh clock signal, and the refresh

controller operable in a low-power mode when the supply voltage is less than or equal to the minimum value to vary the bias voltage as a function of the supply voltage and to generate refresh signals in response to the corresponding refresh clock signal, the refresh signals defining a second refresh rate having a variable value that is a function of the frequency of the refresh clock signal.

18. The refresh controller of claim 17 wherein the refresh controller operates in the low-power mode to vary the bias voltage as a function of the supply voltage to linearly increase the frequency of the refresh clock signal as the supply voltage decreases below the minimum value.

19. The refresh controller of claim 17 wherein the refresh controller generates the bias voltage to develop the refresh clock signal having a substantially constant frequency in the normal mode and generates the bias voltage to increase the frequency of the refresh clock signal as the supply voltage decreases in the low-power mode.

20. The refresh controller of claim 17 wherein the refresh controller generates the bias voltage to develop the refresh clock signal having a substantially constant frequency in the normal mode and outputs the supply voltage as the bias voltage to directly control the frequency of the refresh clock signal as a function of the value of the supply voltage in the low-power mode.

21. The refresh controller of claim 17 wherein the refresh controller generates the bias voltage to develop the refresh clock signal having a substantially constant frequency in the normal mode, and operates in the low-power mode to generate the bias voltage to increase the frequency of the refresh clock signal as the supply voltage decreases when the supply voltage is less than or equal to the minimum value and greater than a second minimum value, and further operates in the low-power mode to output the supply voltage as the bias voltage to directly

control the frequency of the refresh clock signal as a function of the value of the supply voltage when the supply voltage is less than or equal to the second minimum supply value.

22. The refresh controller of claim 17 wherein the integrated circuit is adapted to receive a bias voltage adjustment command that is generated when the refresh controller is to operate in the low-power mode, the command being decoded and applied to the refresh controller which, in response to the decoded command, generates the bias voltage to increase the frequency of the refresh clock signal as the supply voltage decreases.

23. The refresh controller of claim 17 wherein the integrated circuit comprises a dynamic random access memory.

24. A refresh controller for controlling a refresh rate of dynamic data, the refresh controller comprising:

a variable bias voltage generator adapted to receive a supply voltage and operable in a normal mode to generate a bias voltage having a substantially constant value, and operable in a low-power mode to adjust the value of the bias voltage as a function of a magnitude of the supply voltage;

a self-refresh oscillator coupled to the variable bias voltage generator to receive the bias voltage signal, the self-refresh oscillator developing a refresh clock signal having a frequency that is a function of the bias voltage; and

a refresh control circuit coupled to the self-refresh oscillator to receive the refresh clock signal, the refresh control circuit operable in response to the refresh clock signal to develop refresh signals that control the refresh rate of the dynamic data as a function of the frequency of the refresh clock signal.

25. The refresh controller of claim 24 wherein the variable bias voltage generator is operable in the normal mode responsive to the supply voltage being greater than a

minimum value, and is operable in the low-power mode responsive to the supply voltage being less than or equal to the minimum value.

26. The refresh controller of claim 24 wherein the bias voltage generator operates in the low-power mode to adjust the bias voltage as a linear function of the supply voltage.

27. The refresh controller of claim 24 wherein the self-refresh oscillator increases the frequency of the refresh clock signal as the bias voltage decreases and decreases the frequency of the refresh clock signal as the bias voltage increases.

28. The refresh controller of claim 24 wherein the refresh control circuit comprises a self-refresh row and bank address counter operable to generate row and bank addresses responsive to the refresh clock signal, the rate at which the row and bank addresses are generated being a function of the frequency of the refresh clock signal and the refresh rate being a function of the rate at which the row and bank addresses are generated.

29. A refresh controller for controlling a refresh rate of dynamic data, the refresh controller comprising:

a variable bias voltage generator adapted to receive a supply voltage and operable in a normal mode to generate a bias voltage having a substantially constant value, and operable in a low-power mode to output the supply voltage as the bias voltage;

a self-refresh oscillator coupled to the variable bias voltage generator to receive the bias voltage signal, the self-refresh oscillator developing a refresh clock signal having a frequency that is a function of the bias voltage; and

a refresh control circuit coupled to the self-refresh oscillator to receive the refresh clock signal, the refresh control circuit operable in response to the refresh clock signal to develop refresh signals that control the refresh rate of the dynamic data as a function of the frequency of the refresh clock signal.

30. The refresh controller of claim 29 wherein the voltage bias generator operates in the normal mode responsive to the supply voltage being greater than a minimum value, and operates in the low-power mode responsive to the supply voltage being less than or equal to the minimum value.

31. The refresh controller of claim 29 wherein the self-refresh oscillator increases the frequency of the refresh clock signal as the bias voltage increases and decreases the frequency of the refresh clock signal as the bias voltage decreases.

32. The refresh controller of claim 29 wherein the refresh control circuit comprises a self-refresh row and bank address counter operable to generate row and bank addresses responsive to the refresh clock signal, the rate at which the row and bank addresses are generated being a function of the frequency of the refresh clock signal and the refresh rate being a function of the rate at which the row and bank addresses are generated.

33. A refresh controller for controlling a refresh rate of dynamic data in an integrated circuit, the refresh controller comprising:

a variable bias voltage generator adapted to receive a supply voltage and operable in a normal mode to generate a bias voltage having a substantially constant value, and operable in a low-power mode responsive to a bias voltage adjustment command that is generated external to the integrated circuit, the variable bias voltage generator operable in response to the command to adjust the value of the bias voltage as a function of a magnitude of the supply voltage;

a self-refresh oscillator coupled to the variable bias voltage generator to receive the bias voltage signal, the self-refresh oscillator developing a refresh clock signal having a frequency that is a function of the bias voltage; and

a refresh control circuit coupled to the self-refresh oscillator to receive the refresh clock signal, the refresh control circuit operable in response to the refresh clock signal to develop refresh signals that control the refresh rate of the dynamic data as a function of the frequency of the refresh clock signal.

34. The refresh controller of claim 33 wherein bias voltage adjustment command comprises a load mode register command.

35. The refresh controller of claim 33 wherein the variable bias voltage generator is operable in the normal mode responsive to the supply voltage being greater than a minimum value, and is operable in the low-power mode responsive to the supply voltage being less than or equal to the minimum value.

36. The refresh controller of claim 33 wherein the bias voltage generator operates in the low-power mode to adjust the bias voltage as a linear function of the supply voltage.

37. The refresh controller of claim 33 wherein the self-refresh oscillator increases the frequency of the refresh clock signal as the bias voltage decreases and decreases the frequency of the refresh clock signal as the bias voltage increases.

38. The refresh controller of claim 33 wherein the refresh control circuit comprises a self-refresh row and bank address counter operable to generate row and bank addresses responsive to the refresh clock signal, the rate at which the row and bank addresses are

generated being a function of the frequency of the refresh clock signal and the refresh rate being a function of the rate at which the row and bank addresses are generated.

39. A refresh controller for controlling a refresh rate of dynamic data, the refresh controller comprising:

a variable bias voltage generator adapted to receive a supply voltage, the variable bias voltage generator operable in a normal mode to generate a bias voltage having a substantially constant value, and operable in a first low-power mode to adjust the value of the bias voltage as a function of a magnitude of the supply voltage and operable in a second low-power mode to output the supply voltage as the bias voltage;

a self-refresh oscillator coupled to the variable bias voltage generator to receive the bias voltage signal, the self-refresh oscillator developing a refresh clock signal having a frequency that is a function of the bias voltage; and

a refresh control circuit coupled to the self-refresh oscillator to receive the refresh clock signal, the refresh control circuit operable in response to the refresh clock signal to develop refresh signals that control the refresh rate of the dynamic data as a function of the frequency of the refresh clock signal.

40. The refresh controller of claim 39 wherein the variable bias voltage generator is operable in the normal mode responsive to the supply voltage being greater than a first minimum value, and is operable in the first low-power mode responsive to the supply voltage being less than or equal to the first minimum value and greater than a second minimum value, and is operable in the second low-power mode responsive to the supply voltage being less than or equal to the second minimum value.

41. The refresh controller of claim 40 wherein the bias voltage generator operates in the first low-power mode to adjust the bias voltage as a linear function of the supply voltage.

42. The refresh controller of claim 40 wherein the self-refresh oscillator increases the frequency of the refresh clock signal as the bias voltage increases and decreases the frequency of the refresh clock signal as the bias voltage decreases.

43. The refresh controller of claim 40 wherein the refresh control circuit comprises a self-refresh row and bank address counter operable to generate row and bank addresses responsive to the refresh clock signal, the rate at which the row and bank addresses are generated being a function of the frequency of the refresh clock signal and the refresh rate being a function of the rate at which the row and bank addresses are generated.

44. A memory device, comprising:

an address decoder coupled to an address bus;

a read/write circuit coupled to a data bus;

a control circuit coupled to a control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit, the memory-cell array storing dynamic data; and

a refresh controller coupled to the memory-cell array, control circuit and address decoder for controlling a refresh rate of the dynamic data, the refresh controller being adapted to receive a supply voltage and including a refresh oscillator that generates a refresh clock signal having a frequency that is a function of a bias voltage, the refresh circuit operable in a normal mode when the supply voltage is greater than a minimum value to apply a substantially constant bias voltage to the refresh oscillator and to generate refresh signals in response to the corresponding refresh clock signal, the refresh signals defining a first refresh rate having a value determined by the frequency of the refresh clock signal, and the refresh controller operable in a low-power mode when the supply voltage is less than or equal to the minimum value to vary the bias voltage as a function of the supply voltage and to generate refresh signals in response to the corresponding refresh clock signal, the refresh signals defining a second refresh rate having a variable value that is a function of the frequency of the refresh clock signal.

45. The memory device of claim 44 wherein the refresh controller operates in the low-power mode to vary the bias voltage as a function of the supply voltage to linearly increase the frequency of the refresh clock signal as the supply voltage decreases below the minimum value.

46. The memory device of claim 44 wherein the refresh controller generates the bias voltage to develop the refresh clock signal having a substantially constant frequency in the normal mode and generates the bias voltage to increase the frequency of the refresh clock signal as the supply voltage decreases in the low-power mode.

47. The refresh controller of claim 44 wherein the refresh controller generates the bias voltage to develop the refresh clock signal having a substantially constant frequency in the normal mode and outputs the supply voltage as the bias voltage to directly control the frequency of the refresh clock signal as a function of the value of the supply voltage in the low-power mode.

48. The memory device of claim 44 wherein the refresh controller generates the bias voltage to develop the refresh clock signal having a substantially constant frequency in the normal mode, and operates in the low-power mode to generate the bias voltage to increase the frequency of the refresh clock signal as the supply voltage decreases when the supply voltage is less than or equal to the minimum value and greater than a second minimum value, and further operates in the low-power mode to output the supply voltage as the bias voltage to directly control the frequency of the refresh clock signal as a function of the value of the supply voltage when the supply voltage is less than or equal to the second minimum supply value.

49. The refresh controller of claim 44 wherein the memory device is adapted to receive a bias voltage adjustment command that is generated when the refresh controller is to operate in the low-power mode, the command being decoded and applied to the refresh controller

which, in response to the decoded command, generates the bias voltage to increase the frequency of the refresh clock signal as the supply voltage decreases.

50. The memory device of claim 44 wherein the memory device comprises a dynamic random access memory.

51. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device including,

an address decoder coupled to an address bus;

a read/write circuit coupled to a data bus;

a control circuit coupled to a control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit, the memory-cell array storing dynamic data; and

a refresh controller coupled to the memory-cell array, control circuit, and address decoder for controlling a refresh rate of the dynamic data, the refresh controller being adapted to receive a supply voltage and including a refresh oscillator that generates a refresh clock signal having a frequency that is a function of a bias voltage, the refresh circuit operable in a normal mode when the supply voltage is greater than a minimum value to apply a substantially constant bias voltage to the refresh oscillator and to generate refresh signals in response to the corresponding refresh clock signal, the refresh signals defining a first refresh rate having a value determined by the frequency of the refresh clock signal, and the refresh controller operable in a low-power mode when the supply voltage is less than or equal to the minimum value to vary the bias voltage as a function of the supply voltage and to generate refresh signals in response to the corresponding refresh clock signal, the refresh signals defining a second refresh rate having a variable value that is a function of the frequency of the refresh clock signal.

52. The computer system of claim 51 wherein the refresh controller operates in the low-power mode to vary the bias voltage as a function of the supply voltage to linearly increase the frequency of the refresh clock signal as the supply voltage decreases below the minimum value.

53. The computer system of claim 51 wherein the refresh controller generates the bias voltage to develop the refresh clock signal having a substantially constant frequency in the normal mode and generates the bias voltage to increase the frequency of the refresh clock signal as the supply voltage decreases in the low-power mode.

54. The computer system of claim 51 wherein the refresh controller generates the bias voltage to develop the refresh clock signal having a substantially constant frequency in the normal mode and outputs the supply voltage as the bias voltage to directly control the frequency of the refresh clock signal as a function of the value of the supply voltage in the low-power mode.

55. The computer system of claim 51 wherein the refresh controller generates the bias voltage to develop the refresh clock signal having a substantially constant frequency in the normal mode, and operates in the low-power mode to generate the bias voltage to increase the frequency of the refresh clock signal as the supply voltage decreases when the supply voltage is less than or equal to the minimum value and greater than a second minimum value, and further operates in the low-power mode to output the supply voltage as the bias voltage to directly control the frequency of the refresh clock signal as a function of the value of the supply voltage when the supply voltage is less than or equal to the second minimum supply value.

56. The computer system of claim 51 wherein the memory device is adapted to receive a bias voltage adjustment command that is generated when the refresh controller is to operate in the low-power mode, the command being decoded and applied to the refresh controller which, in response to the decoded command, generates the bias voltage to increase the frequency of the refresh clock signal as the supply voltage decreases.

57. The computer system of claim 51 wherein the memory device comprises a dynamic random access memory.